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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/089,907

07/09/2002

Xiaoning Nie

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01/06/2005

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EXAMINER

PAN, DANIEL H

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 01/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/089,907

Applicant(s)

NIE, XIAONING

Examiner

Daniel Pan

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 April 2002.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) 1-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 and 20-24 is/are rejected.
- 7) ☒ Claim(s) 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 April 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>04/05/02</u> . | 6) <input type="checkbox"/> Other: _____  |

1. Claims 1-14 have been canceled. Claims 13-24 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 13-16, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Irwin et al. (5,841,771).

3. As to claim 13, Alpert disclosed a processor system (see fig.2) including at least

:

a) a program memory [main memory] (see the prefetch of instructions from main memory in col.5, lines 24-33);

b) instruction reading means [prefetcher] for reading out the instruction from the memory (see the prefetch of instructions from main memory in col.5, lines 24-33);

c) instruction decoding means [decoder 202] for decoding the instructions (see decoder in col.5, lines 31-33);

d) a plurality of executing units [203][204][205] operable in parallel of various instructions (see parallel execution in col.5, lines 38-41, lines 62-63); and the instruction read out means [prefetcher] and the decoder jointly provided for all execution units (see the prefetch and decoding of the instructions to the execution units in col.5, lines 31-51).

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Alpert did not specifically teach his first bus was slower than the second bus as claimed. However, Irwin disclosed a system including a first bus [header] (see the fifth octet of header occupied 2 times the interval of one octet in col.24, lines 60-67) which had a lower rate than the second bus (see the 4 octets per 25.7ns in col.25, lines 9-13, see also the separate header bus and payload bus in fig.9). It would have been obvious to one of ordinary skill in the art to use Irwin in Alpert for including the slower rate as claimed because the use of Irwing could provide the ability of Alpert to adjust to different rate, thereby increasing the ability to accept a predestined set of clock speed, and one of ordinary skill in the art should be able to recognize the advantage of using variable rate as taught by Irwing into Alpert in order to achieve the enhanced flexibility, and for the above reason provided a motivation.

Alpert is used as primary reference because it showed clearly the plurality of execution units in parallel (see parallel execution in col.5, lines 38-41, lines 62-63).

4. As to claim 14, Alpert also included a temporary storage for storing information required by the execution units (see the data cache 206 in col.5, lines 48-53).

5. As to claim 15, Alpert also included a first execution unit [203] from executing all possible instructions [integer instructions] and a second execution unit [205] for execute only a few instructions (floating point instructions, see col.5, lines 37-50).

6. As to claim 16, the claim language : "execute only one special instruction" is interpreted as the execution of only one special type of instruction because any execution unit is capable of executing only one instruction regardless of the type of

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instruction. Applicant is welcome to provide feedback in ht next response. Albert also execute only one type of instruction (see the FP instruction).

7. As to claim 20, 22, Irwing also included header and payload data (see the separate header bus and payload bus in fig.9), transmitter and I/O ports (see col.22, 23, Table 1).

8. As to claim 21, Irwing also included i/o ports (see col.22, 23, Table 1).

9. As to claim 23, Albert also included first data bus and second data bus (see the input and output connections to the execution units in fig.2 ) .

As to claim 24, Alpert's first execution unit also connected to a second bus (see the output connection from [204] while the second execution unit [205] was only connected to the second data bus (see fig.2).

10. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alpert et al. (5,559,986) in view Irwin et al. (5,841,771) as applied to claims 13,14,15,16 above, and further in view of Berg (4,196,470).

11. As to claim 17, neither Alpert nor Irwin specifically showed the move instruction for move a data block as claimed. However, Berg disclosed one instruction for transferring data block (e.g. see col.3, lines 38-46). It would have been obvious to one of ordinary skill in the art to use Berg in Albert for including move instruction as claims

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because the use of Berg could provide the control capability of Alpert to adapt to specific type of data transfer based on a predetermined instruction format, such as a move instruction, and therefore, increasing the adaptability of the execution unit of Alpert, and because Alpert did show an offset values for a data block to be transferred (see the byte boundary in col.10, lines 1-2), which was a suggestion of the need of using an instruction for moving data block, and it could be achieved by configuring the control parameters of the move instruction (e.g. the transfer instruction type, and the instruction width) into Alpert so that move instruction was implementable in Alpert to achieve the enhance control, in doing so, provided a motivation.

12. As to claim 18, Alpert also included a storage or loading address of a data block to be stored or loaded, the amount of data elements, an offset value for storage or reading out (see the detailed references of the data line and size in the data cache memory in col.6, lines 39-67, col.7, lines 1-24, see also col.8, lines 21-42, col.9, lines 8-33, see the byte boundary for the offset value in col.10, lines 1-2).

13. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the path leading to the first execution unit was temporarily deactivated by the instruction read out means via the decoding means if momentarily no instruction had to be executed by the first execution unit.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

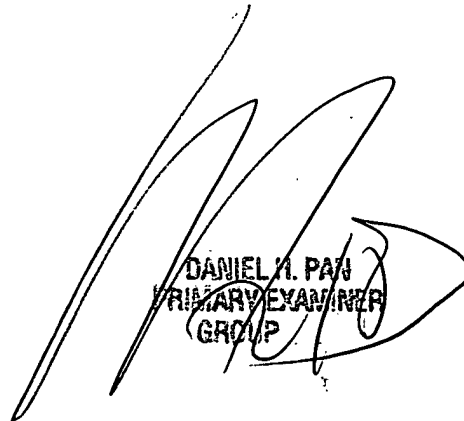
a) Harriman, Jr. et al. (5,442,750) is cited for the background teaching in transmitter and receiver and the header bus and the data bus (see col.3, lines 16-45, see also fig.1B).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*21 Century Strategic Plan*

  
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